IMPROVED COMPUTER-AIDED SYNTHESIS TOOLS FOR THE DESIGN OF MATCHING NETWORKS FOR WIDEBAND MICROWAVE AMPLIFIERS

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ABSTRACT---Network synthesis is a powerful design tool when applied to the design of matching networks for wideband microwave amplifiers. Significant design improvements have been made in the computer-aided synthesis process which provides a powerful, efficient and friendly tool for the microwave amplifier designer. Design methodologies are given, computer automation methods outlined and a complete amplifier design example is included.

A. INTRODUCTION

Network synthesis has long been a workhorse tool for the design of low-frequency and microwave filters. In recent years, it has begun to be applied to the problem of wideband matching networks for microwave amplifiers[1-2] via extensions of classical synthesis techniques. This paper describes significant improvements in the synthesis of matching networks for wideband amplifiers and in the automation thereof. The key improvements are:

1. A simplified and automated method of modeling device impedances.
2. A methodology for selecting topologies that meet parasitic inclusion and impedance transformation requirements which is efficiently automated.
3. An automated method for adjusting the gain-bandwidth and selecting reflection coefficient zeros consistent with parasites to be included.

These improvements provide a powerful, friendly and useful tool for the microwave amplifier designer.

In Section B, the synthesis design process as applied to wideband matching networks is outlined with attention called to the steps which have been significantly improved via the techniques described in this paper.

Sections C, D, and E describe in detail the areas of improved design methods in the matching network synthesis process.

Section F describes a complete microwave amplifier design using the design techniques of this paper.

Section G summarizes the results and benefits possible using the design methodologies of this paper.

B. STEPS IN THE MATCHING NETWORK SYNTHESIS PROCESS

The steps in matching network synthesis are outlined in Figure 1 and listed here. Steps shown with an (*) indicate areas in which significant improvements have been made via the techniques described in the following sections.

*1. Model the input and output impedance of the active devices to be used in the microwave amplifier.
*2. Select a topology consistent with device parasitics.
*3. Adjust the gain-bandwidth to insure inclusion of parasitics.
*4. Select the reflection coefficient zeros consistent with inclusion of parasitics.
5. Transform impedances to desired levels.
6. Transform the lumped design to a transmission line realization.
7. Analyze the resultant design by itself and/or as part of the complete amplifier design.
8. Optimize the amplifier design (if needed).

C. A SIMPLIFIED AND AUTOMATED METHOD OF MODELING DEVICE IMPEDANCES

The input and output impedances of active devices have generally been modeled by curve-fitting, optimization or Smith Chart manipulation. A simpler algebraic method which provides very satisfactory accuracy and greatly improved speed

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and convenience is achieved by using the simple impedance models shown in Figure 2. The modeled element values are then obtained by applying the following constraints to the three different types of circuits:

Circuit Type	Constraint at f_u (upper passband edge)	Constraint at f_1 (lower passband edge)
- Two Element Networks	- Exact agreement with measured impedance; both real and imaginary parts	- None
- Three Element Series -Series or Shunt-Shunt type	- Exact agreement of both real and imaginary parts	- Agreement of imaginary parts
- Three Element Series Shunt Type	- Exact agreement of both real and imaginary parts	- Agreement of real parts

Then the behavior of the model at f_1 is compared to the device impedance from measured S-parameters. From the networks which yield a realizable network, the impedance model which has the greatest accuracy at f_1 is chosen. The degree of accuracy of the model at f_1 is obtained by simply computing the resultant model behavior at f_1, comparing to the actual Z behavior at f_1 and computing the potential matching error due to modelling inaccuracy.

This method yields very accurate results with quite simple models. An application example is given with the amplifier design of Section F.

An example of the resulting equations from applying the outlined constraints is as follows:

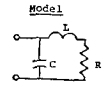
Measured Impedance

$$z = \frac{(1 + S_{ii})}{(1 - S_{ii})} z_0 \qquad i = 1 \text{ for Input}, \; i = 2 \text{ for Output}$$

$$z = R_u + jX_u = \frac{1}{G_u + jB_u} \quad @ \; f = f_u$$

$$z = R_1 + jX_1 = \frac{1}{G_1 + jB_1} \quad @ \; f = f_1$$

Model



Resulting Equations

$$R = \frac{(1/G_u - (f_u/f_1)^2/G_1)}{1 - (f_u/f_1)^2} \qquad (1)$$

$$L = \frac{\sqrt{R/G_u - R^2}}{2\pi f_u} \qquad (2)$$

$$C = \frac{B_u + (2\pi f_u L)/(R^2 + (2\pi f_u L)^2}{2\pi f_u} \qquad (3)$$

D. SIMPLIFIED AND AUTOMATED SELECTION OF TOPOLOGIES FOR MATCHING NETWORK SYNTHESIS

Topology selection has been a stumbling block in matching network synthesis for the following reasons:

- Many topologies are available which provide a valid result even after parasitic constraints are applied.
- Topologies vary in their ability to provide impedance transformations and there is no known way to predict the impedance-transforming capability of a network before it is synthesized.

Given then that many topologies are available and that there are no known a-priori methods for selecting a good topology, the following options were considered in an effort to more efficiently select topologies:

METHOD 1) Allow (require) the designer to try various topologies and manually select the one which meets his parasitic inclusion and impedance transformation requirements: This has been the traditional approach but is extremely inefficient on the time (and patience) of the microwave designer.

METHOD 2) Have the computer search through all possible topologies and select out those topologies which meet parasitic inclusion and impedance transformation requirements. This is much more efficient than 1) since the elimination of invalid topologies is done by the computer. However, the topology search and eliminate process must be done each and every time the designer performs a synthesis and it still leaves the user to select among the valid topologies that are left.

METHOD 3) Do an a-priori study to determine good default topologies for specific combinations of parasitics that need to be included on each side of the network. A good topology would accommodate the existent parasitics and provide a wide range of impedance transformation capability. This method provides for the simplest selection of a default topology for the user and would execute in the minumum possible time.

METHOD 3) was selected as the best tradeoff for synthesis of matching networks. Therefore, a study was made to determine which topologies provided a wide range of impedance transformation for a given set of parasitics at each end of the matching network. Several general conclusions were drawn from this study:

1. The impedance transforming capability of a matching network is most strongly dependent upon the topology itself and much less strongly dependant upon the frequency response specification. This discovery makes METHOD 3) very workable since default topologies can be selected based upon the requisite parasitic in-

clusion requirements without regard to the specific frequency response specification.

2. Sufficient flexibility is obtained for matching network topologies without requiring networks any higher than six reactive elements. In fact, fourth order networks are often quite satisfactory in obtaining the requisite bandwidth, parasitic inclusion capability, and impedance transformation. For automation simplicity, all default topologies were chosen to be sixth order matching networks.

An example default topology is given here:

Parasitic Inclusion			Approximate Impedance Transforming Range	
@ Input	@ Output	Good Default Topology	Minimum	Maximum
CP	LS	CP LP LS CP CS LS	1 : 0.054	1 : 5.4

E. IMPROVED AND AUTOMATED METHODS OF ADJUSTING THE GAIN-BANDWIDTH AND SELECTING REFLECTION COEFFICIENT ZEROS TO ASSURE INCLUSION OF PARASITIC ELEMENTS

The gain-bandwidth of a synthesis has to be constrained and the reflection coefficients have to be selected (either left half plane or right half plane) properly in order to assure that existent parasitics can be included into synthesized networks. This can be a tedious manual process to adjust the gain, try all combinations of reflection zeros....especially for a microwave designer unfamiliar with synthesis theory.

The approach taken here is to automate the gain-bandwidth adjustment and reflection zero process in the following way:

1. From a given frequency response specification (set by the user), automatically adjust the gain (if and only if necessary) to assure parasitic inclusion and save all solutions that meet the parasitic inclusion requirements. This provides a set of several valid solutions that can be quickly stepped through and selected by the user.
2. The method of gain adjustment is a binary search on the gain parameter whereby:
   a) A maximum allowable gain is first tested to see if it meets the parasitic requirements (e.g. 1 dB).
   b) Then half maximum is tested.
   c) Depending on the results of a) and b), either 1/4 maximum or 3/4 maximum is tested.
   d) The process continues until the difference between successive successful tests is sufficiently small (e.g. 0.1 dB).

This method is very efficient because the binary search algorythm converges quite rapidly and because the testing for parasitic inclusion can be obtained with straight-forward calculations.

3. The designer is not bothered with the inner workings of the synthesis computations. Rather, the designer specifies requirements such as frequency response, parasitics to be included, source and terminating resistance and is then presented alternative solutions which can be quickly scanned for selection.

F. COMPLETE AMPLIFIER DESIGN USING THE TECHNIQUES OF THIS PAPER

AMPLIFIER SPECIFICATIONS : 15 db +- 2 dB over 6-12 GHz

TRANSISTOR : The (chip) Hp GaAs FET whose parameters are listed in Figure 3.

TRANSISTOR MODELLING : The transistor is shown modelled in Figure 4 using a computer-aided implementation of the techniques of this paper.

MATCHING NETWORK SPECIFICATIONS :

	Gain Slope	Ripple	Parasitics To Be Included	
Input	6 dB/Oct	.4 dB		FET I/P
Interstage	6 dB/Oct	.4 dB	FET O/P	FET I/P
Output	0	.04 dB	FET O/P	

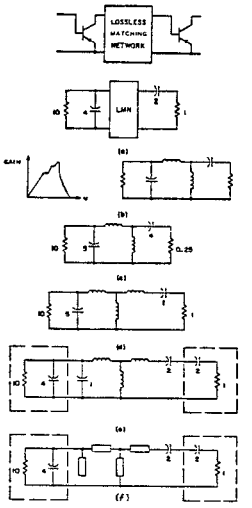
The computer-aided design of these networks is shown in Figure 5.

ANALYSIS OF COMPLETE AMPLIFIER

Figure 6 and 7 show the analysis of the complete amplifier response. This response is exactly as designed without optimization. Deviations from ideal expectations exist due to the fact that the transistors are not unilateral ($S_{12} \neq 0$) and due to the fact that the transmission-line realization is not an exact representation of the lumped design. Overall, the results are a very good first-cut design and could be improved further through optimization.

G. SUMMARY

Simplified and improved synthesis techniques coupled with automation of the same provides a powerful and useable tool in the design of wideband matching networks for microwave amplifiers.



(a) Model Device Impedances

(b) – Constrain Frequency Response and Select Topology Consistent with Parasitic Elements
– Select reflection coefficient zeros

(c) Synthesize Network

(d) Transform Impedance

(e) Separate Out Device Impedances

(f) Transform Design to Approximated Transmission-Line Equivalent

Figure 1. Outline of the Process of Synthesis of Matching Networks for Microwave Amplifiers.

a) Input Network

```
# ELEMENTS =   4.000 # HI PASS =    2.000  SOLUTION  2  / 4     : TEE TRANSFORM
SOURCE RES.=  50.000 DES. LOAD =   11.400 Flower=      6.000 Fupper=      12.000
SLOPE =        6.000 RIPPLE =      0.400 MIN LOSS =   0.000  SHAPE=   ER
ZERO LOCATIONS : COMPLEX ZEROS :  0  0
 SYNTHESIZED NETWORK     : IMP TRANSFORMED NET :          TRANS LINE NETWORK
**************************************************************************
  SOURCE    50.0000  OHM SOURCE    50.0000  OHM SOURCE    50.0000  OHM
  1 CP       0.470743 pF  CP       0.470743 pF  TLOC    41.584 DEG  25 OHMS
  2 LP       1.015955 nH  LS       0.301762 nH  TLIN    10.736 DEG 120 OHMS
  3 LS       1.612095 nH  LP       0.714195 nH  TLSC    24.168 DEG 120 OHMS
  4 CS       0.142697 pF  LS       0.584527 nH  TLIN    20.167 DEG 120 OHMS
  5LOAD     23.068667 OHM CS       0.538218 pF  CS
  6                       CS       0.622000 pF  CS       0.622000 pF
  7                     LOAD      11.400000 OHMLOAD     11.400000 OHM
**************************************************************************
```

b) Interstage Network

```
# ELEMENTS =   4.000 # HI PASS =    2.000  SOLUTION  2  / 4     : TEE TRANSFORM
SOURCE RES.= 123.600 DES. LOAD =   11.400 Flower=      6.000 Fupper=      12.000
SLOPE =        6.000 RIPPLE =      0.400 MIN LOSS =   0.000  SHAPE=   ER
ZERO LOCATIONS : COMPLEX ZEROS :  0  0
 SYNTHESIZED NETWORK     : IMP TRANSFORMED NET :          TRANS LINE NETWORK
**************************************************************************
  SOURCE   123.6000  OHM SOURCE   123.6000  OHM SOURCE   123.6000  OHM
  1 CP       0.190430 pF  CP       0.168000 pF  CP       0.168000 pF
  2 LP       2.511440 nH  LS       0.022430 pF  TLOC     2.421 DEG  25 OHMS
  3 LS       3.985094 nH  LS       1.388544 nH  TLIN    41.103 DEG 120 OHMS
  4 CS       0.057725 pF  LP       1.122897 nH  TLSC    33.204 DEG 120 OHMS
  5LOAD     57.025745 OHM LS       0.175824 nH  TLIN     6.204 DEG 120 OHMS
  6                       CS       0.528143 pF  CS       0.528143 pF
  7                       CS       0.622100 pF  CS       0.622100 pF
  8                     LOAD      11.400000 OHMLOAD     11.400000 OHM
**************************************************************************
```

c) Output Network

```
# ELEMENTS =   4.000 # HI PASS =    2.000  SOLUTION  2  / 2     : TEE TRANSFORM
SOURCE RES.= 127.600 DES. LOAD =   50.000 Flower=      6.000 Fupper=      12.000
SLOPE =        0.000 RIPPLE =      0.040 MIN LOSS =   0.063  SHAPE=   EF
ZERO LOCATIONS : COMPLEX ZEROS :  I  I
 SYNTHESIZED NETWORK     : IMP TRANSFORMED NET :          TRANS LINE NETWORK
**************************************************************************
  SOURCE   127.6000  OHM SOURCE   127.6000  OHM SOURCE   127.6000  OHM
  1 CP       0.186480 pF  CP       0.168900 pF  CP       0.168000 pF
  2 LP       1.886579 nH  CP       0.018480 pF  TLOC     1.995 DEG  25 OHMS
  3 LS       1.253654 nH  LS       0.486986 nH  TLIN    17.013 DEG 120 OHMS
  4 CS       0.290627 pF  LP       1.399592 nH  TLSC    41.328 DEG 120 OHMS
  5LOAD     90.848230 OHM LS       0.328692 nH  TLIN    11.669 DEG 120 OHMS
  6                       CS       0.509890 pF  CS       0.509890 pF
  7                     LOAD      50.000000 OHMLOAD     50.000000 OHM
**************************************************************************
```

Figure 5. Synthesis of Matching Networks.

a) Two Element Models

b) Three Element Series-Series or Shunt-Models

c) Three Element Shunt-Series Models

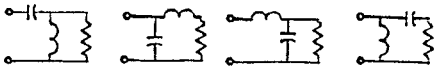
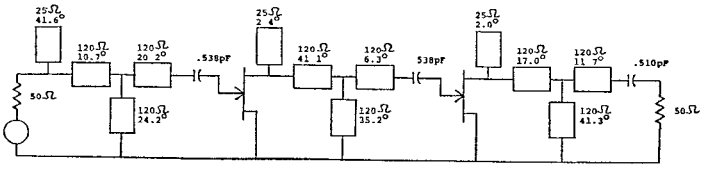


Figure 2. Simple Impedance Models for Modelling Active Device Impedances.



Note : Electrical Degrees are at $f_u = GH_z$.

Figure 6. Completed Two Stage GaAs FET Amplifier.

FREQ-GHZ	MAG[S11] FET	ANG[S11] FET	DB[S21] FET	ANG[S21] FET	MAG[S12] FET	ANG[S12] FET	MAG[S22] FET	ANG[S22] FET
6.00000	0.769	-97.000	8.855	104.000	0.049	39.000	0.486	-48.000
7.00000	0.741	-107.500	7.924	96.000	0.071	35.500	0.482	-54.500
8.00000	0.713	-118.000	6.884	88.000	0.077	32.000	0.480	-61.000
9.00000	0.708	-122.500	5.872	82.000	0.070	31.000	0.498	-65.500
10.0000	0.703	-127.000	4.926	76.000	0.067	30.000	0.515	-70.000
11.0000	0.691	-129.500	3.946	72.500	0.067	31.500	0.540	-70.500
12.0000	0.678	-132.000	3.088	69.000	0.066	33.000	0.564	-71.000

Figure 3. S-parameters of HP GaAs FET used in Amplifier Design Example.

```
SPARAMETER DATA USED FOR MODEL :
    F(GHz)   S11MAG     S11ANG     S21MAG     S22MAG     S22ANG
     6.000    0.769     -97.000     2.771      0.486     -48.000
    12.000    0.678    -132.000     1.427      0.564     -71.000

ELEMENT VALUES ARE IN  Ohms  pF  nH

BEST 2-ELEMENT MODEL FOR S 1  1
    CS          R
  0.6231     11.4134
FIT IS EXACT AT Fupper. . . .ERROR AT Flower =          0.413  %
APPROXIMATE WORST CASE ERROR IN dB =                    0.027  dB

BEST 2-ELEMENT MODEL FOR S 2  2
    CP          R
  0.1679    123.5758
FIT IS EXACT AT Fupper. . . .ERROR AT Flower =         18.413  %
APPROXIMATE WORST CASE ERROR IN dB =                    0.734  dB

AVAILABLE GAIN AT Flower =                             13.910  dB
AVAILABLE GAIN AT Fupper =                              7.425  dB
GAIN ROLLOFF =                                          6.485  dB
GAIN ROLLOFF =                                          6.485  dB/Oct
SELECT A SOFTKEY COMMAND ?
```

Figure 4. FET Gain and Impedance Modelling.

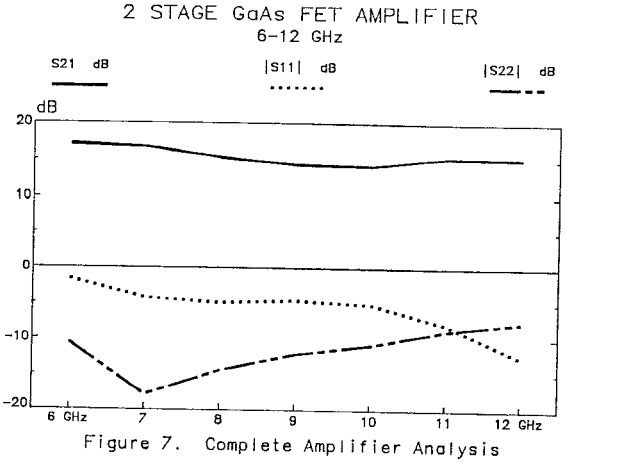


Figure 7. Complete Amplifier Analysis